Amendments to the claims:

1 (currently amended): A method of grouping cells for scan testing comprising steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) initializing a corresponding list of cells for each of a plurality of common signal domains in the integrated circuit design, each corresponding list of cells created as an empty list;

(c) selecting a cell in ~~that belongs to~~ one of the common signal domains ~~and~~ that is not included in a corresponding list of cells for any of the common signal domains;

(d) tracing a net from an input port of the selected cell to a signal driver;

(e) inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver;

(f) tracing the net to an input port of each cell connected to the signal driver; and

(g) inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver.

2 (previously presented): The method of Claim 1 further comprising a step of repeating steps (c), (d), (e), (f), and (g) until every cell belonging to the common signal domain associated with the signal driver has been inserted in the corresponding list of cells for the common signal domain associated with the signal driver.

3 (previously presented): The method of Claim 2 further comprising a step of generating as output the corresponding list of cells for each of the plurality of common signal domains in the integrated circuit design.

4 (previously presented): The method of Claim 1 wherein step (e) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver.

5 (previously presented): The method of Claim 1 comprising performing steps (b), (c), (d), (e), (f), and (g) for cells comprising flip-flops in a scan chain.

6 (previously presented): The method of Claim 5 comprising performing steps (b), (c), (d), (e), (f), and (g) for one of the common signal domains that is a scan clock domain.

7 (previously presented): The method of Claim 6 comprising performing steps (d), (e), (f), and (g) for a net that is a clock net.

8 (previously presented): The method of Claim 7 comprising performing steps (d), (e), (f), and (g) for an input port that is a clock port.

9 (previously presented): The method of Claim 8 comprising performing steps (d), (e), (f), and (g) for a signal driver that is a clock driver.

10 (currently amended): A computer readable storage medium tangibly embodying instructions for a computer that when executed by the computer implement a method ~~program product~~ for grouping cells for scan testing, the method comprising ~~a computer readable medium embodying a computer program for input to a computer, the computer program, when executed by the computer, causing the computer to perform~~ steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) initializing a corresponding list of cells for each of a plurality of common signal domains in the integrated circuit design, each corresponding list of cells created as an empty list;

(c) selecting a cell in ~~that belongs to~~ one of the common signal domains ~~and~~ that is not included in a corresponding list of cells for any of the common signal domains;

(d) tracing a net from an input port of the selected cell to a signal driver;

(e) inserting the selected cell in the corresponding list of cells for the common signal

domain associated with the signal driver;

(f) tracing the net to an input port of each cell connected to the signal driver; and

(g) inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver.

11 (currently amended): The computer readable storage medium ~~program product~~ of Claim 10 further causing the computer to perform a step of repeating steps (c), (d), (e), (f), and (g) until every cell belonging to the common signal domain associated with the signal driver has been inserted in the corresponding list of cells for the common signal domain associated with the signal driver.

12 (currently amended): The computer readable storage medium ~~program product~~ of Claim 11 further causing the computer to perform a step of generating as output the corresponding list of cells for each of the plurality of common signal domains in the integrated circuit design.

13 (currently amended): The computer readable storage medium ~~program product~~ of Claim 10 wherein step (e) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver.

14 (currently amended): The computer readable storage medium ~~program product~~ of Claim 10 further causing the computer to perform steps (b), (c), (d), (e), (f), and (g) for cells comprising flip-flops in a scan chain.

15 (currently amended): The computer readable storage medium ~~program product~~ of Claim 14 further causing the computer to perform steps (b), (c), (d), (e), (f), and (g) for one of the common signal domains that is a scan clock domain.

16 (currently amended): The computer readable storage medium ~~program product~~ of Claim 15 further causing the computer to perform steps (d), (e), (f), and (g) for a net that is a clock net.

17 (currently amended): The computer readable storage medium ~~program product~~ of Claim 16 further causing the computer to perform steps (d), (e), (f), and (g) for an input port that is a clock port.

18 (currently amended): The computer readable storage medium ~~program product~~ of Claim 17 further causing the computer to perform steps (d), (e), (f), and (g) for a signal driver that is a clock driver.

19 (new): A method of grouping cells for scan testing comprising steps of:

receiving as input a representation of an integrated circuit design that includes cells clocked by a corresponding clock signal driver for one of a plurality of common clock signal domains;

initializing a corresponding list of cells for each of the common clock signal domains by creating each corresponding list of cells as an empty list;

selecting a cell having a clock signal input that is not included in a corresponding list of cells for any of the common clock signal domains;

tracing a net from the clock signal input of the selected cell to the corresponding clock signal driver;

inserting the selected cell in the corresponding list of cells for the common clock signal domain associated with the clock signal driver;

tracing the net from the clock signal input of the selected cell to a clock signal input of each cell connected to the clock signal input of the selected cell; and

inserting each cell traced from the selected cell in the corresponding list of cells for the common clock signal domain clocked by the corresponding clock signal driver.

20 (new): A computer readable storage medium tangibly embodying instructions for a computer that when executed by the computer implement a method for grouping cells for scan testing, the method comprising steps of:

receiving as input a representation of an integrated circuit design that includes cells clocked by a corresponding clock signal driver for one of a plurality of common clock signal domains;

initializing a corresponding list of cells for each of the common clock signal domains by creating each corresponding list of cells as an empty list;

selecting a cell having a clock signal input that is not included in a corresponding list of cells for any of the common clock signal domains;

tracing a net from the clock signal input of the selected cell to the corresponding clock signal driver;

inserting the selected cell in the corresponding list of cells for the common clock signal domain associated with the clock signal driver;

tracing the net from the clock signal input of the selected cell to a clock signal input of each cell connected to the clock signal input of the selected cell; and

inserting each cell traced from the selected cell in the corresponding list of cells for the common clock signal domain clocked by the corresponding clock signal driver.